2305

Lead-free

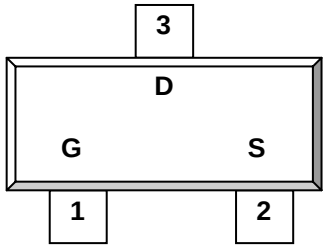
P Channel Enhancement Mode MOSFET

-3.5A

DESCRIPTION

2305 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION
SOT-23

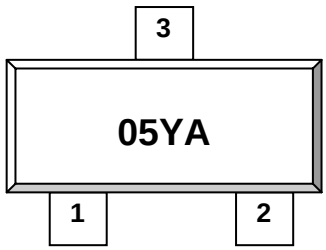


1.Gate 2.Source 3.Drain

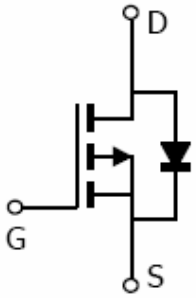
FEATURE

- -15V/-3.5A, $R_{DS(ON)}$ = 63m-ohm (Typ.) @VGS = -4.5V
- -15V/-3.0A, $R_{DS(ON)}$ = 80m-ohm @VGS = -2.5V
- -15V/-2.0A, RDS(ON)= 90m-ohm @VGS=-1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PART MARKING
SOT-23



Y: Year Code A: Process Code



ORDERING INFORMATION

Part Number	Package	Part Marking
2305SRG	SOT-23	05YA

※ Process Code：A ~ Z ; a ~ z

※ 2305SRG S：SOT23 ; R：Tape Reel ; G：Pb – Free

-3.5A

ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

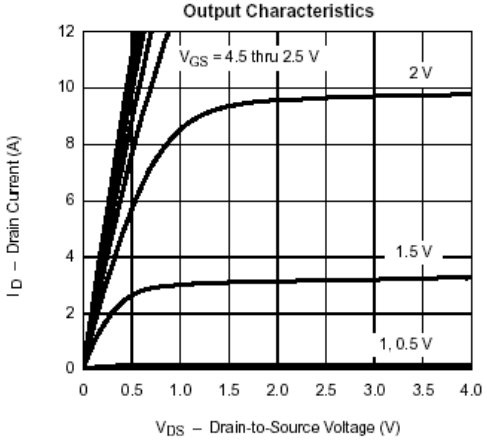
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-15	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain CurrentTJ=150℃)	T_A=25℃ T_A=70℃	I_D	-3.5 -2.8	A
Pulsed Drain Current		I_{DM}	-10	A
Continuous Source Current (Diode Conduction)		I_S	-1.6	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	120	℃/W

ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

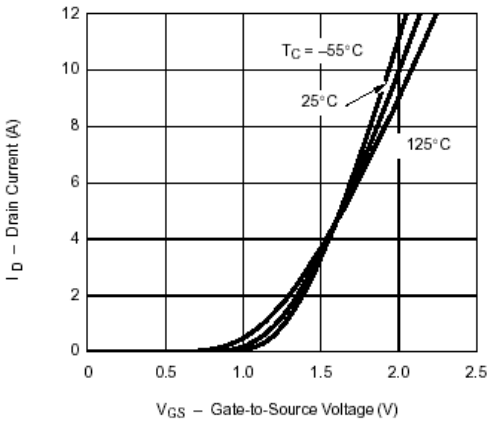
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250uA	-15			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS, I_D=-250uA	-0.3		-1.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V			-1	uA
		V_{DS}=-20V, V_{GS}=0V T_J=55℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V, V_{GS}=-4.5V V_{DS}≦-5V, V_{GS}=-2.5V	-6 -3			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V, I_D=-3.5A V_{GS}=-2.5V, I_D=-3.0A V_{GS}=-1.8V, I_D=-2.0A		0.063 0.080 0.090		Ω
Forward Transconductance	g_{fs}	V_{DS}=-5V, I_D=-3.5V		8.5		S
Diode Forward Voltage	V_{SD}	I_S=-1.6A, V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-10V V_{GS}=-4.5V I_D≡-3.5A		10	12	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2		
Input Capacitance	C_{iss}	V_{DS}=-10V V_{GS}=0V F=1MHz		485		pF
Output Capacitance	C_{oss}			90		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$	V_{DD}=-10V R_L=6Ω I_D=-1.0A V_{GEN}=-4.5V R_G=6Ω		10	18	nS
	t_r			13	22	
Turn-Off Time	$t_{d(off)}$			18	24	
	t_f			15	20	

TYPICAL CHARACTERICTICS (25℃ Unless noted)

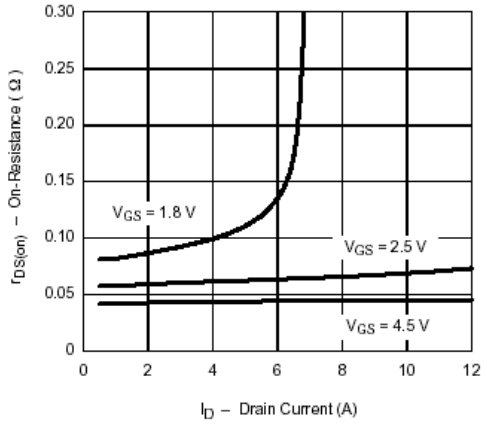
Output Characteristics



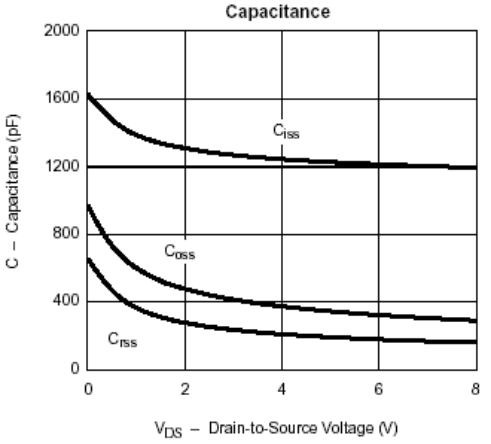
Transfer Characteristics



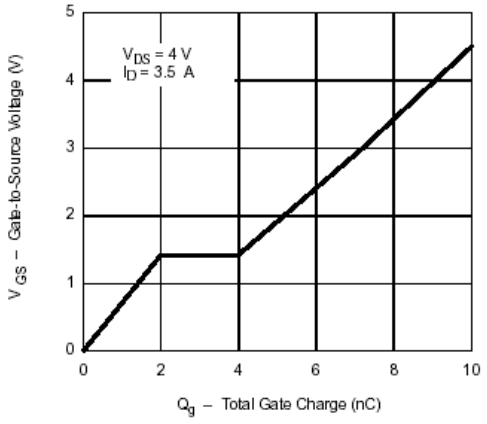
On-Resistance vs. Drain Current



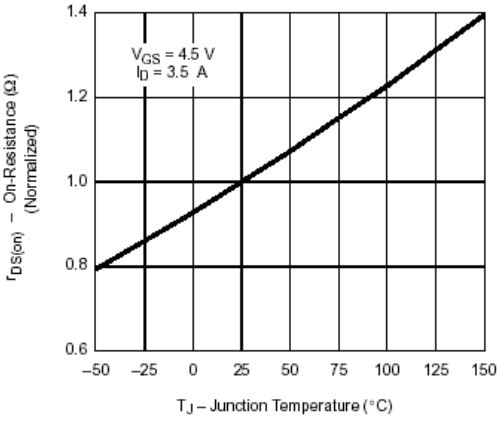
Capacitance



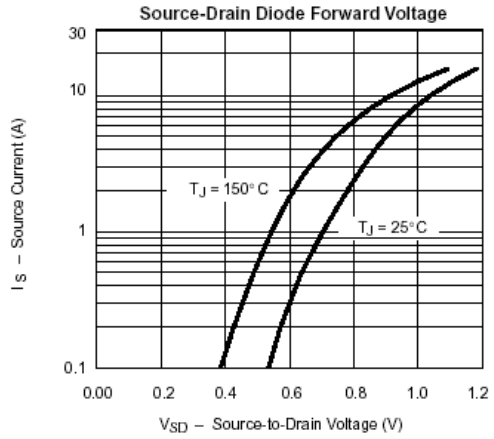
Gate Charge

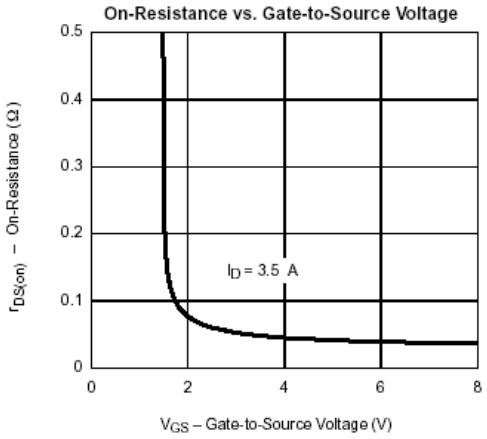


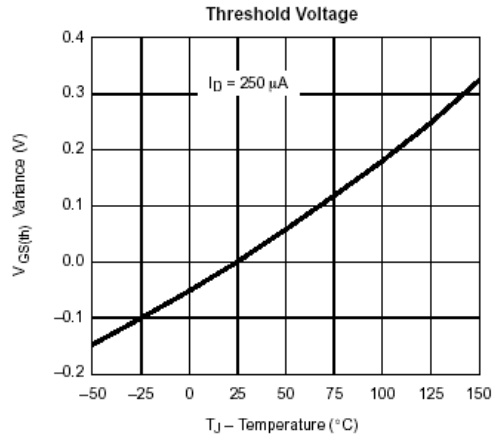
On-Resistance vs. Junction Temperature

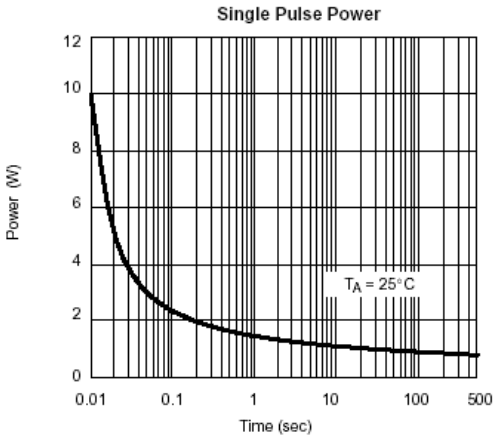


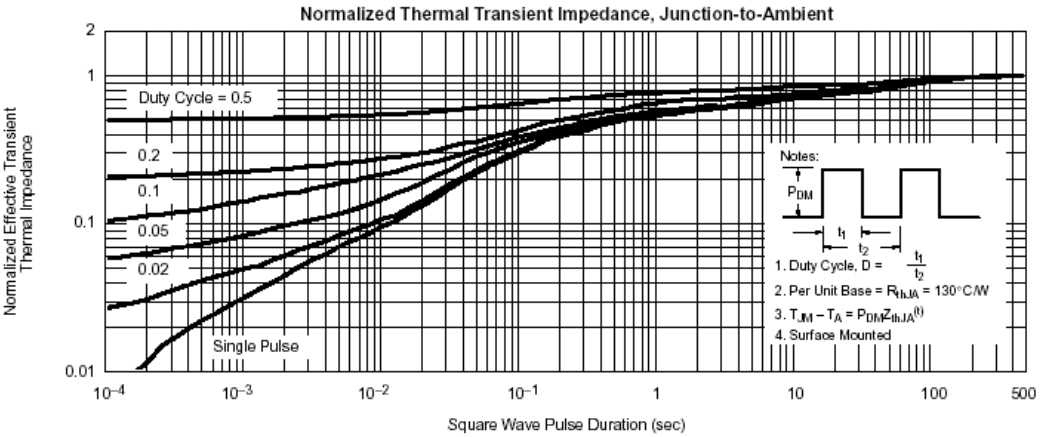
TYPICAL CHARACTERICTICS (25℃ Unless noted)



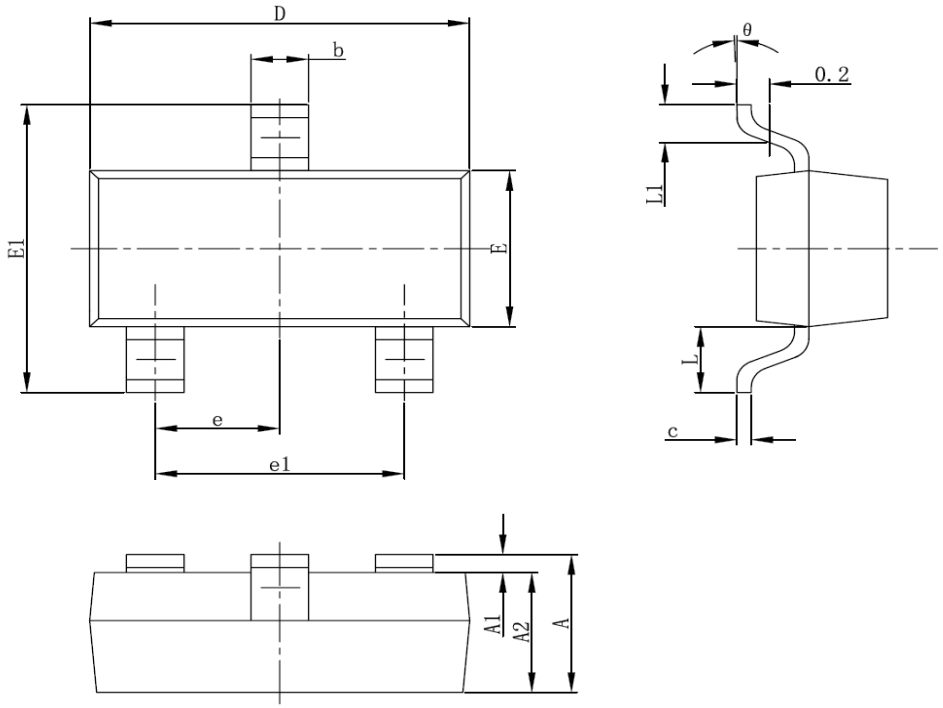








SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°