

2303SRG



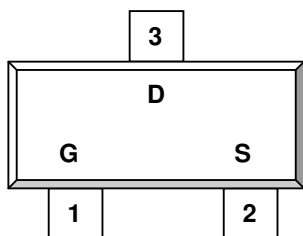
P Channel Enhancement Mode MOSFET

-2.6A

DESCRIPTION

2303SRG is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION SOT-23

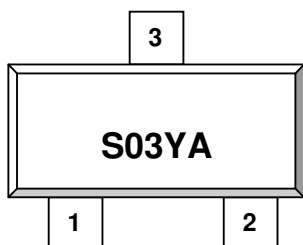


1.Gate 2.Source 3.Drain

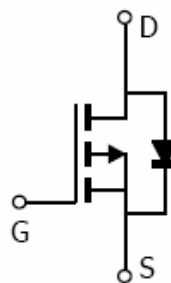
FEATURE

- -30V/-2.6A, $R_{DS(ON)} = 95\text{m-ohm}$ (Typ.) @VGS = -10V
- -30V/-2.0A, $R_{DS(ON)} = 125\text{m-ohm}$ @VGS = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PART MARKING SOT-23



Y: Year Code A: Process Code



2303SRG

P Channel Enhancement Mode MOSFET

-2.6A**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	-30	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	T _A =25°C T _A =70°C	I _D	-2.6 -2.0	A
Pulsed Drain Current		I _{DM}	-10	A
Continuous Source Current (Diode Conduction)		I _S	-1.25	A
Power Dissipation	T _A =25°C T _A =70°C	P _D	1.25 0.8	W
Operation Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	100	°C/W

2303SRG

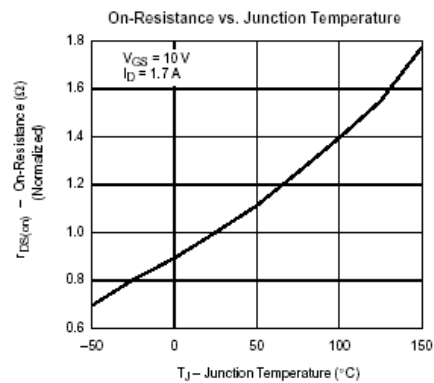
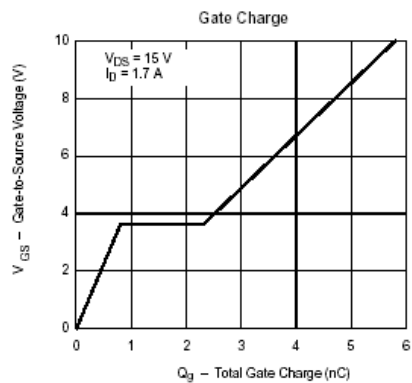
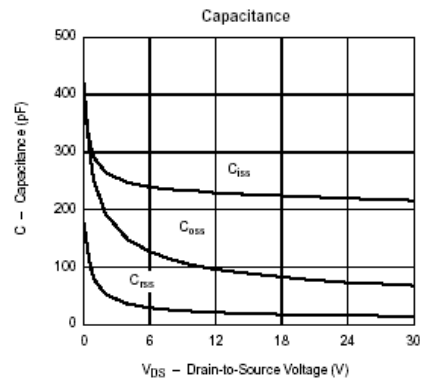
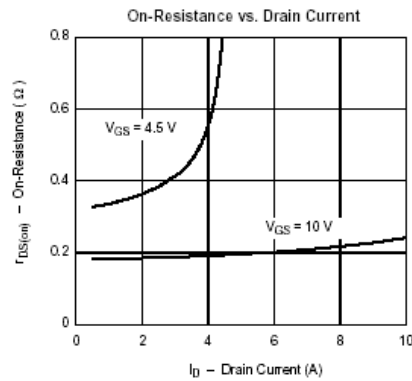
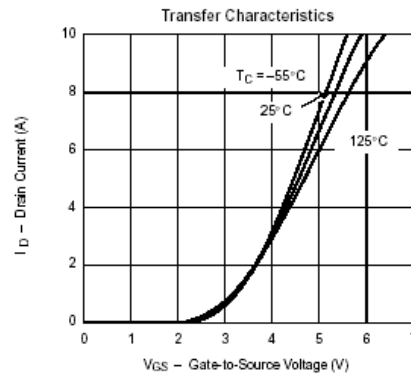
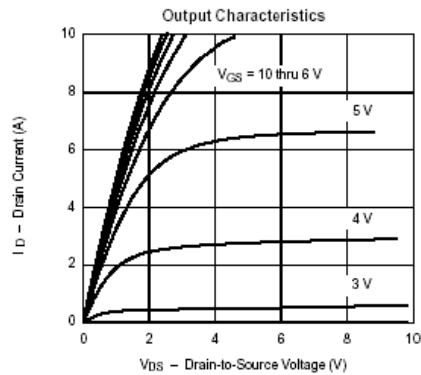
P Channel Enhancement Mode MOSFET

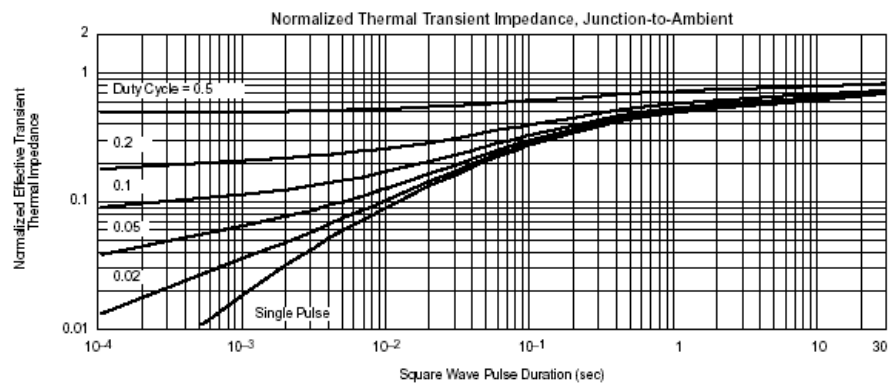
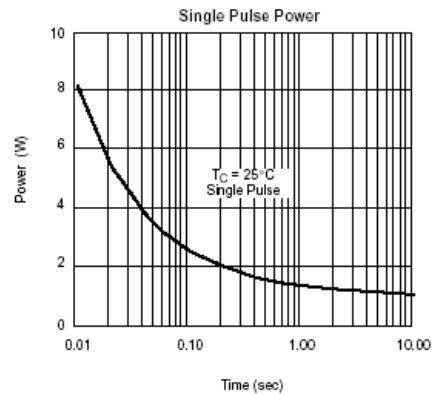
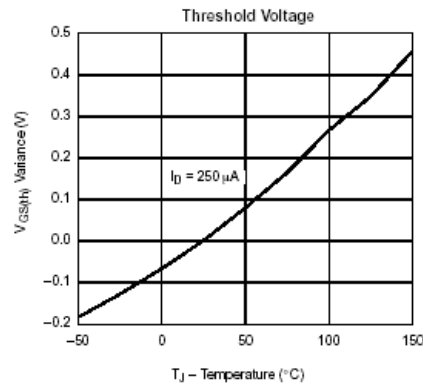
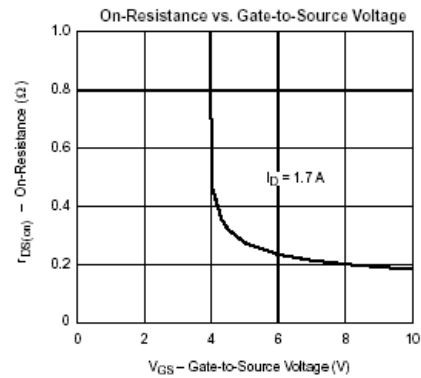
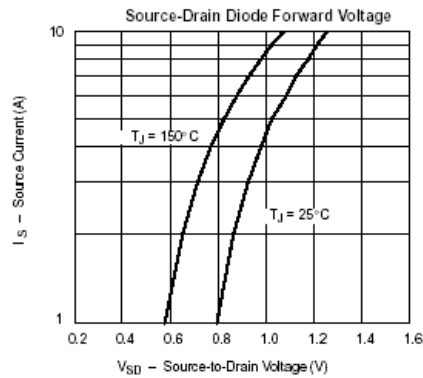
-2.6A**ELECTRICAL CHARACTERISTICS** (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V,I _D =-10uA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250uA	-1.0		-3.0	V
Gate Leakage Current	I _{GSS}	V _{DS} =0V,V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V,V _{GS} =0V			-1	uA
		V _{DS} =-30V,V _{GS} =0V T _J =55℃			-10	
Drain-source On-Resistance	R _{DS(on)}	V _{GS} =-10V,I _D =-2.6A V _{GS} =-4.5V,I _D =-2.0A		0.095 0.125		Ω
Forward Transconductance	g _{fs}	V _{DS} =-10V,I _D =-1.7V		2.4		S
Diode Forward Voltage	V _{SD}	I _S =-1.25A,V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-15V V _{GS} =-10V I _D ≡-1.7A		5.8	10	nC
Gate-Source Charge	Q _{gs}			0.8		
Gate-Drain Charge	Q _{gd}			1.5		
Input Capacitance	C _{iss}	V _{DS} =-15V V _{GS} =0V F=1MHz		226		pF
Output Capacitance	C _{oss}			87		
Reverse Transfer Capacitance	C _{rss}			19		
Turn-On Time	t _{d(on)} tr	V _{DD} =-15V R _L =15Ω I _D =-1.0A V _{GEN} =-10V R _G =6Ω		9	20	nS
				9	20	
Turn-Off Time	t _{d(off)} tf			18	35	
				6	20	

2303SRG

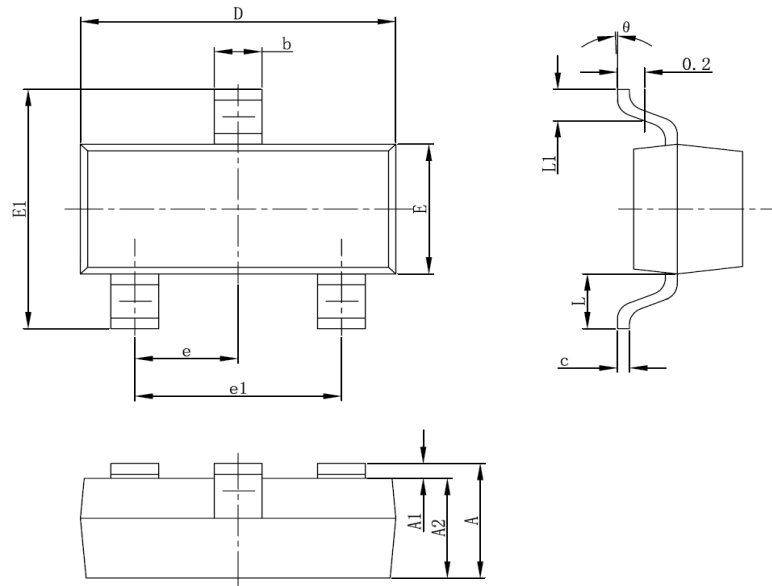
P Channel Enhancement Mode MOSFET

-2.6A**TYPICAL CHARACTERISTICS** (25°C Unless noted)

TYPICAL CHARACTERISTICS (25°C Unless noted)

2303SRG

P Channel Enhancement Mode MOSFET

-2.6A**SOT-23 PACKAGE OUTLINE**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°